WHAT IS CLAIMED IS:

1. A GPS RF Front End integrated within a wireless mobile terminal, the GPS RF Front End containing a Frequency Synthesizer comprising:

a Voltage Controlled Oscillator (VCO) for producing a Local Oscillator (LO) signal, wherein the LO signal has a frequency at approximately 1566 MHz;

a first fixed counter means, coupled to the VCO, for dividing the LO signal frequency by 41, to obtain a second signal with frequency of LO/41, wherein the second signal is an ACQCLK signal;

a second fixed counter means, coupled to the VCO, for dividing the LO signal by 31-and-8/9ths, to obtain a third signal with frequency of 9/7 times the frequency of the second signal, wherein the second signal is a GPSCLK signal, the second fixed counter means further comprising a first divide-by-4 counter, the first divide-by-4 counter having five outputs, each output having a frequency of LO/4;

a second divide-by-4 counter, coupled to one of the five outputs of the first divide-by-4 counter;

a first programmable count-down counter, coupled to the output of the second divide-by-4 counter;

a second programmable count-down counter, coupled to a Reference Frequency Signal, the Reference Frequency Signal being used by the wireless mobile terminal; and

a Phase Frequency Detector, coupled to the outputs of the first and second programmable count-down counters, for comparing the phase and frequency of the outputs of the first and second programmable count-down counters.

2. The GPS RF Front End of claim 1, wherein the first counter means comprises:

a divide-by-3/4 counter; and

a divide-by-11 counter, coupled to the output of the divide-by-3/4 counter, wherein the LO signal, the output of the divide-by-3/4, and the output of the divide-by-11 counter assist in the generation of a select control signal to determine the divide ratio of the divide-by-3/4 counter.

3. The GPS RF Front End of claim 1, wherein the first counter means comprises:

a divide-by-4 counter for producing four quadrature signals each having frequency LO/4,

a 4:1 mux, coupled to the divide-by-4 counter;

a divide-by-10 counter coupled to a output of 4:1 mux output; and

a state register for controlling a phase selection state of the 4:1 mux.